REMARKS

Claims 1-26 are now pending in the application. Claim 1 has been amended, according to the Examiner's suggestions, to cure the informalities objected to. New Claims 20-26 have sufficient basis in the original detailed description. The amendments to the claims contained herein are of equivalent scope as originally filed, and thus are not a narrowing amendment. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art in view of Farrer et al., U.S. Patent 5,307,320. This rejection is respectfully traversed.

Claim 1 recites that a storage control "activates the current switch command at a predetermined time later than the preceding switch command." It also recites that "information items allocated to the storage cells are capable of being supplied to the storage control, which information items indicate the predetermined time mentioned." Farrer discloses a timing field which includes three discrete timing parameters. Instead of supplying the time between the current switch command and a preceding switch command, Farrer allows for only three very specific and limited timing fields. The ability to supply a set of predetermined times between the current switch command and a previous switch command enables the present invention to work with a wide variety of memory types. In contrast, Farrer will only work with a subset of DRAM memories. Furthermore, the timing parameter fields of Farrer offer only a limited number of choices

for the three timing parameters that can be altered. It is not obvious to extend the limited configurability of Farrer to the finely programmable architecture of the present invention which allows the use of the storage control with a number of memory types.

Referring to Claims 2-19, applicant respectfully disagrees that the Examiner's prior art combination teaches all limitations. Claims 2-5 recite a way in which a switch command can be activated at a specified time after a previous switch command. Farrer does not allow for arbitrary spacing of switch commands, and thus the present invention as claimed would be undesirable for Farrer because of its added complexity and cost. Further, Farrer does not teach or suggest any such claimed subject matter.

The new access signal recited by Claim 9 is not referred to or necessary in Farrer. As such, Claim 9 is not taught or suggested by Farrer.

Claim 19 recites "information items allocated to the storage cells also give the time, after which after activating the first switch command of each new command sequence, the writing or reading respectively is concluded." The Examiner asserts that "the concluded time is given since the registers give the time required to remain active for some signals." Farrer allows setting active times for only two signals: RAS and CAS. More importantly, the times of Claim 19 are from activation of the first switch command until conclusion of the access. These are much different than simply the time for a certain signal to be active.

Claim 13 recites a "write/read memory or a programmable read only memory into which the switch commands are written in an initializing process." Farrer discloses no initializing process because the switch commands in the invention of Farrer are predetermined, and only a select few parameters are variable. Farrer does not need

new switch commands, since it works only with DRAM memories. Farrer simply provides variables to alter the behavior of some of the predetermined switch commands.

Claim 15 recites that "the command set is determined for each respective storage type by means of information items allocated to the storage cells." There is only one command set offered in the invention of Farrer, and therefore Farrer can not suggest nor disclose determining command sets for different storage types.

The amended Claim 1 now includes the limitation "that the storage control contains command sets for several different storage types." An additional limitation is "that a single command set can be determined by the information items." Farrer is not capable of containing command sets for several different storage types. The invention in Farrer is amenable only to a subset of DRAM memories that can be controlled within the limited flexibility of Farrer. Applicant respectfully asserts that Claim 1 and those claims dependent upon it (2-19) are now in condition for allowance.

Claims 20-24 have been added. For the same reasons as above, Claims 20-24 are neither disclosed nor suggested by Farrer. Claim 20 recites that memory control commands and information are "programmable into the register depending upon the type of memory being utilized." As stated above, Farrer does not allow new memory control commands to be programmed, allowing Farrer to only control a select set of DRAM memories. Instead of providing a few variables to control a pre-programmed DRAM sequence, the present invention allows a generic architecture of memory control commands to be programmed into the register to control a wide variety of memory types.

Claims 21-24 depend upon Claim 20, and the Applicant respectfully asserts that they are therefore also in condition for allowance.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed or accommodated. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: July 13, 2004

By: _____
G. Gregory Schivley
Reg. No. 27,382

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

[GGS/mrn]